

IN THE CLAIMS

Please amend claim 68 as follows below.

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1 1. (Original) A method of processing for a semiconductor device, the method
2 comprising:
3 providing a wafer including a substrate;
4 forming a plurality of sidewalls around a plurality of cylindrical pedestals above a
5 surface of the substrate;
6 removing the plurality of cylindrical pedestals; and
7 vertically etching horizontal surfaces of a first material located around the
8 plurality of sidewalls.

1 2. (Original) The method of claim 1, wherein,
2 the plurality of sidewalls provide an etch stop.

1 3. (Original) The method of claim 2, wherein,
2 the plurality of sidewalls protect the first material under the plurality of sidewalls
3 from being etched during the vertical etching of the first material.

1 4. (Original) The method of claim 1, further comprising:
2 removing the plurality of sidewalls.

1 5. (Original) The method of claim 1, further comprising:

2 diffusing a dopant into the first material located around the plurality of sidewalls.

1 6. (Original) The method of claim 1, further comprising:

2 diffusing a dopant into a second material around the plurality of sidewalls.

1 7. (Original) The method of claim 1, further comprising:

2 diffusing a dopant into the first material and a second material around the plurality
3 of sidewalls.

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1 8. (Original) The method of claim 1, further comprising:

2 diffusing a dopant into the first material or a second material around the plurality
3 of sidewalls.

1 9. (Original) The method of claim 8, wherein,

2 the plurality of sidewalls provide an etch stop and a diffusion barrier.

1 10. (Original) The method of claim 9, wherein,

2 the plurality of sidewalls protect the first material under the plurality of sidewalls
3 from receiving a dopant during the diffusing of the dopant into the first material or the
4 second material.

1 11. (Original) The method of claim 9, wherein,

2 the plurality of sidewalls protect the second material under the plurality of
3 sidewalls from receiving a dopant during the diffusing of the dopant into the first material
4 and the second material.

1 12. (Original) The method of claim 9, wherein,
2 the plurality of sidewalls protect the first material and the second material under
3 the plurality of sidewalls from receiving a dopant during the diffusing of the dopant into
4 the first material or the second material.

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1 13. (Original) A method of processing for a semiconductor device, the method
2 comprising:
3 providing a wafer including a substrate;
4 forming a plurality of sidewalls around a plurality of cylindrical pedestals above a
5 surface of the substrate;
6 removing the plurality of cylindrical pedestals; and
7 diffusing a dopant into a first material located around the plurality of sidewalls.

1 14. (Original) The method of claim 13, wherein,
2 the plurality of sidewalls provide a diffusion barrier.

1 15. (Original) The method of claim 14, wherein,
2 the plurality of sidewalls protect the first material under the plurality of sidewalls
3 from receiving a dopant during the diffusing of the dopant into the first material.

1 16. (Original) The method of claim 13, further comprising:
2 removing the plurality of sidewalls.

1 17. (Original) The method of claim 13, further comprising:

2 vertically etching horizontal surfaces of the first material located around the
3 plurality of sidewalls.

1 18. (Original) The method of claim 13, further comprising:
2 vertically etching horizontal surfaces of a second material located around the
3 plurality of sidewalls.

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1 19. (Original) The method of claim 13, further comprising:
2 vertically etching horizontal surfaces of the first material and a second material
3 located around the plurality of sidewalls.

1 20. (Original) The method of claim 13, further comprising:
2 vertically etching horizontal surfaces of the substrate located around the plurality
3 of sidewalls.

1 21. (Original) The method of claim 13, further comprising:
2 vertically etching horizontal surfaces of the first material or a second material
3 located around the plurality of sidewalls.

1 22. (Original) The method of claim 21, wherein,
2 the plurality of sidewalls provide a diffusion barrier and an etch stop.

1 23. (Original) The method of claim 22, wherein,
2 the plurality of sidewalls protect the first material under the plurality of sidewalls
3 from being etched during the etching of the first material.

1 24. (Original) The method of claim 22, wherein,
2 the plurality of sidewalls protect the second material under the plurality of
3 sidewalls from being etched during the etching of the second material.

1 25. (Original) The method of claim 22, wherein,
2 the plurality of sidewalls protect the first material and the second material under
3 the plurality of sidewalls from being etched during the vertical etching of the first
4 material and the second material.

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1 26. (Original) The method of claim 22, wherein,
2 the plurality of sidewalls protect the first material or the second material under the
3 plurality of sidewalls from being etched during the vertical etching of the first material or
4 the second material.

1 27. (Original) A method of processing for a semiconductor device, the method
2 comprising:
3 providing a substrate of the semiconductor device;
4 forming a plurality of sidewalls above a surface of the substrate;
5 vertically etching horizontal surfaces of a material located around the plurality of
6 sidewalls; and
7 diffusing a dopant around the plurality of sidewalls.

1 28. (Original) The method of claim 27, wherein,
2 the plurality of sidewalls are formed by

3 forming a plurality of cylindrical pedestals above a surface of the
4 substrate,
5 depositing a sidewall material layer over the cylindrical pedestals and the
6 substrate,
7 vertically etching the horizontal surfaces of the sidewall material, and
8 etching away the plurality of cylindrical pedestals.

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1 29. (Original) The method of claim 27, wherein,
2 the vertical etching of horizontal surfaces of the material located around the
3 plurality of sidewalls is performed using a substantially anisotropic etchant.

1 30. (Original) The method of claim 27, wherein,
2 the plurality of sidewalls provide an etch stop and a diffusion barrier.

1 31. (Original) The method of claim 30, wherein,
2 the plurality of sidewalls protect the material under the plurality of sidewalls from
3 being etched during the etching of the material around the plurality of sidewalls and the
4 plurality of sidewalls protect the material under the plurality of sidewalls from receiving
5 the dopant during the diffusing of the dopant around the plurality of sidewalls.

1 32. (Original) A method of processing for a semiconductor device, the method
2 comprising:
3 providing a substrate of the semiconductor device;
4 forming a plurality of sidewalls above a surface of the substrate; and
5 diffusing a dopant around the plurality of sidewalls.

1 33. (Original) The method of claim 32, wherein,
2 the plurality of sidewalls provide a diffusion barrier.

1 34. (Original) The method of claim 32, wherein,
2 the plurality of sidewalls are formed by
3 forming a plurality of cylindrical pedestals above a surface of the
4 substrate,
5 depositing a sidewall material layer over the cylindrical pedestals and the
6 substrate,
7 vertically etching the horizontal surfaces of the sidewall material, and
8 etching away the plurality of cylindrical pedestals.

1 35. (Original) The method of claim 32, further comprising:
2 vertically etching horizontal surfaces of a material located around the plurality of
3 sidewalls.

1 36. (Original) The method of claim 35, wherein,
2 the plurality of sidewalls provide an etch stop and a diffusion barrier.

1 37. (Original) The method of claim 35, wherein,
2 the vertical etching of horizontal surfaces of the material located around the
3 plurality of sidewalls is performed using a substantially anisotropic etchant.

1 38. (Original) The method of claim 36, wherein,

2 the plurality of sidewalls protect the material under the plurality of sidewalls from
3 being etched during the vertical etching of horizontal surfaces of the material around the
4 plurality of sidewalls and the plurality of sidewalls protect the material under the plurality
5 of sidewalls from receiving the dopant during the diffusing of the dopant around the
6 plurality of sidewalls.

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1 39. (Original) The method of claim 35, wherein,
2 the material located around the plurality of sidewalls which is vertically etched is
3 the substrate.

1 40. (Original) The method of claim 35, wherein,
2 the material located around the plurality of sidewalls which is vertically etched is
3 a layer exposed over a surface of the substrate and protected under the plurality of
4 sidewalls.

1 41. (Original) A method of processing for a semiconductor device, the method
2 comprising:
3 providing a substrate of the semiconductor device;
4 forming a plurality of sidewalls above a surface of the substrate; and
5 vertically etching horizontal surfaces of a material located around the plurality of
6 sidewalls.

1 42. (Original) The method of claim 41, wherein,
2 the plurality of sidewalls provide an etch stop.

1 43. (Original) The method of claim 41, wherein,

2 the material located around the plurality of sidewalls which is horizontally etched
3 is the substrate.

1 44. (Original) The method of claim 41, wherein,
2 the material located around the plurality of sidewalls which is horizontally etched
3 is an epitaxial layer of the substrate.

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1 45. (Original) The method of claim 41, wherein,
2 the material located around the plurality of sidewalls which is horizontally etched
3 is a layer exposed over a surface of the substrate and protected under the plurality of
4 sidewalls.

1 46. (Original) The method of claim 41, wherein,
2 the vertical etching of horizontal surfaces of the material located around the
3 plurality of sidewalls is performed using a substantially anisotropic etchant.

1 47. (Original) The method of claim 41, wherein,
2 the plurality of sidewalls are formed by
3 forming a plurality of cylindrical pedestals above a surface of the
4 substrate,
5 depositing a sidewall material layer over the cylindrical pedestals and the
6 substrate,
7 vertically etching the horizontal surfaces of the sidewall material, and
8 etching away the plurality of cylindrical pedestals.

1 48. (Original) The method of claim 41, further comprising:

2 diffusing a dopant around the plurality of sidewalls.

1 49. (Original) The method of claim 48, wherein,
2 the plurality of sidewalls provide an etch stop and a diffusion barrier.

1 50. (Original) The method of claim 49, wherein,
2 the plurality of sidewalls protect the material under the plurality of sidewalls from
3 being etched during the vertical etching of the material located around the plurality of
4 sidewalls and the plurality of sidewalls protect the material under the plurality of
5 sidewalls from receiving the dopant during the diffusing of the dopant around the
6 plurality of sidewalls.

1 51. (Original) The method of claim 48, wherein,
2 the dopant is diffused into the substrate around the plurality of sidewalls.

1 52. (Original) The method of claim 48, wherein,
2 the dopant is diffused into the material around the plurality of sidewalls.

1 53-57. (Cancelled)

1 58. (Original) A system for manufacturing a semiconductor device comprising:
2 a container for receiving a semiconductor wafer;
3 the semiconductor wafer having a plurality of sidewalls formed over a substrate;
4 a means for etching a material around the plurality of sidewalls; and
5 wherein the plurality of sidewalls provide an etch stop to protect the material
6 underneath the plurality of sidewalls from being etched.

1 59. (Original) The system of claim 58, wherein,
2 the means for etching the material is a gas, plasma, or liquid.

1 60. (Original) The system of claim 58, wherein,
2 the means for etching includes an excitation field to excite ions in a gas, plasma,
3 or liquid.

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1 61. (Original) The system of claim 58, further comprising:
2 a means for diffusing dopants into a material around the plurality of sidewalls; and
3 wherein the plurality of sidewalls provide a diffusion barrier to protect the
4 material underneath the plurality of sidewalls from being implanted.

1 62. (Original) The system of claim 61, wherein,
2 the means for diffusing dopants in the material is a gas, plasma, or liquid.

1 63. (Original) The system of claim 58, wherein,
2 the container is a chamber, an oven, or a bath tub.

1 64. (Original) A system for manufacturing a semiconductor device comprising:
2 a container for receiving a semiconductor wafer;
3 the semiconductor wafer having a plurality of sidewalls formed over a substrate;
4 a means for diffusing a dopant into a material around the plurality of sidewalls;
5 and
6 wherein the plurality of sidewalls provide a diffusion barrier to protect the
7 material underneath the plurality of sidewalls from being implanted.

1 65. (Original) The system of claim 64, wherein,
2 the means for diffusing dopants into the material is a gas, plasma, or liquid.

1 66. (Original) The system of claim 64, wherein,
2 the means for diffusing includes an excitation field to implant the dopant into the
3 material around the plurality of sidewalls.

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1 67. (Original) The system of claim 64, wherein,
2 the means for diffusing includes a source of heat to diffuse the dopant into the
3 material around the plurality of sidewalls.

1 68. (Currently Amended) The system of claim ~~64~~ 67, wherein,
2 the source of heat is an oven.

1 69. (Original) The system of claim 64, further comprising:
2 a means for etching into a material around the plurality of sidewalls; and
3 wherein the plurality of sidewalls provide an etch stop to protect the material
4 underneath the plurality of sidewalls from being etched.

1 70. (Original) The system of claim 69, wherein,
2 the means for etching the material is a gas, plasma, or liquid.

1 71. (Original) The system of claim 70, wherein,
2 the means for etching includes an excitation field to excite ions in a gas, plasma,
3 or liquid.

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- 1 72. (Original) The system of claim 71, wherein,
 - 2 the container is a chamber, an oven, or a bath tub.
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